#2. Priority K Jones 3/22/02

INVESTOR IN PEOPLE

The Patent Office
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Newport
South Wales
NP10 8QQ

JC978 U.S. PTO
10/037571
11/09/01

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Request for grant of a patent

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15 NOV 2000

The Patent Office
Cardiff Road
Newport
Gwent NP9 1RH

1. Your reference

GW-G30482

15NOV00 E583764-1 000346
P01/7700 0.00-0027810.1

2. Patent application number
(The Patent Office will fill in this part)

0027810.1

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

Pace Micro Technology Plc

Victoria Road
Saltaire
Shipley
BD18 3LF

Patents ADP number *(if you know it)*

If the applicant is a corporate body, give the country/state of its incorporation

75885 69001

England

4. Title of the invention

Signal Sequencing Control Means

5. Name of your agent *(if you have one)*

Bailey Walsh & Co.

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

5, York Place
Leeds
LS1 2SD

Patents ADP number *(if you know it)*

224001 ✓

6. If you are declaring priority from one or more earlier patent applications, give the and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number

Country	Priority application number *(if you know it)*	Date of filing *(day / month / years)*

7. If this application is divided or otherwise derived from an earlier UK application, the earlier application

Number of earlier application	Date of filing *(day / month / years)*

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer "Yes" if:*

Yes

a) any applicant named in part 3 is not an inventor, or

b) there is an inventor who is not named as an applicant, or

c) any named applicant is a corporate body

See note (d)

9. Enter the number of sheets for any of the following items you are filing with this form. Do not count copies of the same document.

Continuation sheets of this form	
Description	5
Claim(s)	
Abstract	
Drawing(s)	1

10. If you are also filing any of the following, state how many of each item.

Priority Documents	
Translations of priority documents	
Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	
Request for preliminary examination and search *(Patents Form 9/77)*	
Request for substantive examination *(Patents Form 10/77)*	
Any other documents *(Please specify)*	

11. I/We request the grant of a patent on the basis of this application

Signature

Date **14.11.00**

12. Name and daytime telephone number of person to contact in the United Kingdom

G Wood
0113 2433824

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Signal Sequencing Control Means

This invention relates to signal sequencing control means.

Although the following description refers almost exclusively to the use of signal sequencing control means for a smart card, it will be appreciated by persons skilled in that art that the present invention can be used for the control of any signal sequence which needs to be reversed between switching signals on and switching signals off.

Smart cards are the common name given to cards, typically of credit card dimensions, containing a microchip and are used in a variety of applications including securing internet transactions, credit card use, enabling financial transactions, application of ticketing and reward schemes, set top boxes to allow customers to receive and decrypt broadcast signals, for pay-to view channels and/or the like. Smart cards are deemed to be enabled when read in a correct manner by a smart card reader and this requires the sequence of control signals to be enabled in a first order on 'power-up' of the smart card. When use is completed, the sequence of control signals needs to be disabled in a reverse order on 'power-down' of the smart card.

Conventionally the forward and reverse sequences of a smart card are provided by a standard integrated electronic circuit which includes digital timing means to allow the signals in a particular direction to be activated/deactivated at spaced time intervals. In addition, the electronic circuit is provided with two separate paths to drive the power up and power down signals respectively.

Since smart cards and other electronic devices are becoming increasingly used for both business, leisure and personal

pursuits, there is a requirement to make the technology as inexpensive as possible.

An aim of the present invention is to provide a signal sequencing control means which provides an inexpensive and simple solution to activation and deactivation of a sequence of signals.

According to a first aspect of the present invention there is provided a signal sequencing control means for an electronic device, said sequencing control means including an electronic circuit and timing means, to allow a sequence of control signals to be activated in a pre-determined order for operation of the device and deactivated in a reverse order for disabling the device and wherein the electronic circuit is driven to generate the sequence of control signals in a forward and reverse direction along the same circuit path.

Preferably each control signal is controlled by a resistor/capacitor combination and the signals are controlled by a network of said resistor/capacitor combinations to allow the signals to be activated/deactivated in sequence at pre-determined time intervals.

Preferably the number of resistor/capacitor combinations corresponds to the number of signals to be activated/deactivated in the sequence.

Preferably the resistors of the network are provided in series.

Preferably the sequence of control signals are being operated via a number of logic gates.
Further preferably the logic gates are Schmidt Logic Gates.

In one embodiment a logic gate drives voltage through the resistors in a first direction via a diode at the start of the resistor path. A reverse diode is typically provided at the end of the resistor path to drive voltage through the resistors in the reverse direction.

In one embodiment the sequence of the signals in a forwards direction may be different to the sequence of signals in the reverse direction, yet still be driven using the same circuit path.

In one embodiment the electronic device is a smart card. The smart card typically contains four lines which need to be enabled in a correct sequence for the smart card to operate. The four lines allow the supply of voltage to the card, place the bi-directional data line of the card in receive mode, apply the clock, and finally enable the reset signal.

According to a second aspect of the present invention there is provided a signal sequencing control means for a smart card interface, said interface including an electronic circuit and timing means to allow a sequence of control signals to be activated in a pre-determined order for operation of the card and deactivated in a reverse order for disabling the card and wherein the electronic circuit is driven to generate the sequence of control signals in a forwards and reverse direction along the same circuit path.

An advantage of the present invention is that the signal sequencing control means uses a single circuit to drive the sequence of signals in both a forwards and reverse direction. Thus fewer components are required for the signal sequence and the electronic circuitry is therefore inexpensive. This is in contrast to conventional signal sequence control means in which two separate paths and, as a result different sets of components,

are required to drive a sequence of signals in a forward and reverse direction respectively. Conventional circuitry is more expensive than the present invention as more components are required.

An embodiment of the present invention will now be described with reference to the accompanying figure wherein:

Figure 1 is a circuit diagram according to the present invention.

Referring to figure 1, there is illustrated a circuit 2 comprising a first control line 4 and four further lines 6, 8, 10. When the voltage in control line 4 moves from a low condition to a high condition, a timed sequence of signals is initiated in the further lines 6, 8, 10 to enable the circuit.

Firstly, the first logic gate 14 of control line 4 is enabled via diode 16. The combination of resistor 18 and capacitor 20 provides a time delay before the second logic gate 22 of the sequence is enabled. The combination of resistor 24 and capacitor 26 provides a time delay before the third logic gate 28 of the sequence is enabled. Finally the combination of resistor 30 and capacitor 32 provides a time delay before the fourth logic gate 34 of the sequence is enabled.

When the voltage in control line 4 moves from a high condition to a low condition, the timed sequence is reversed and the circuit is disabled. This is a result of voltage passing through diode 36, which disables the fourth gate 34. The combination of resistor 30 and capacitor 26 then disable the third gate 28 after a timed delay. The combination of resistor 24 and capacitor 20 then disable the second gate 22 after a timed delay and finally the combination of resistor 18 and capacitor 38 then disable the first gate 14 after a timed delay.

The circuit described above can be used as part of a smart card interface. A smart card typically contains four lines which need to be enabled in a correct sequence for the smart card to operate. The four lines allow the supply of voltage to the card, place the bi-directional data line of the card in receive mode, apply the clock, and finally enable the reset signal. To safely disable the card after use, the reset signal must be moved from a high condition to a low condition, the clock then needs to be stopped, the data line needs to be moved from a high condition to a low condition and then finally the voltage supply to the

The logic gates 14, 22, 28 and 34 are typically Schmidt gates.

Thus it can be seen that the above system can be used in a number of different electronic devices in which a sequence of control signals needs to be enabled in a first order and disabled in a reverse order.

Although the illustrated circuit shows only 4 lines, it will be appreciated by persons skilled in the art that the circuit can be adapted to include different numbers of lines by increasing or reducing the number of combinations of capacitors and resistors.

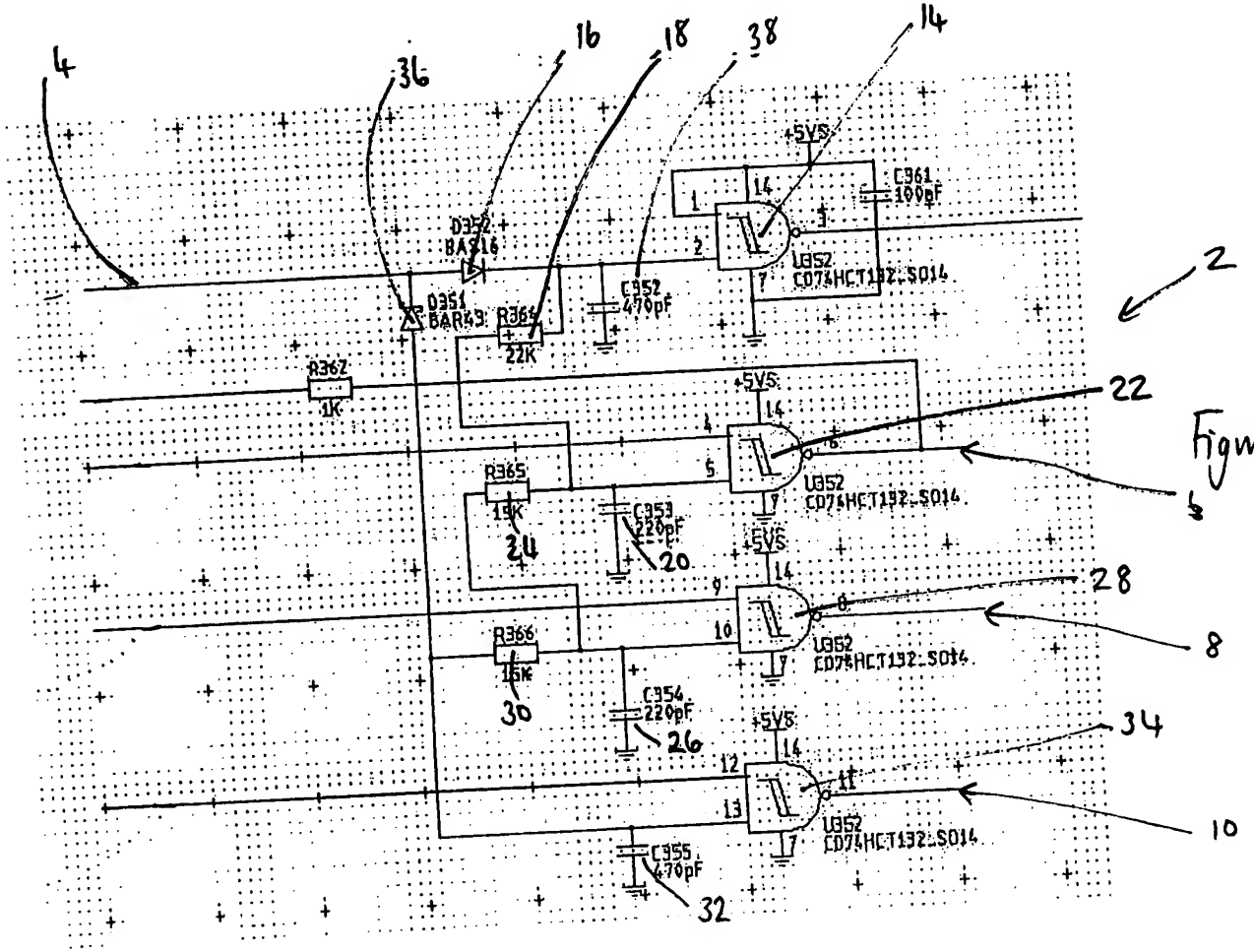
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Figure 1

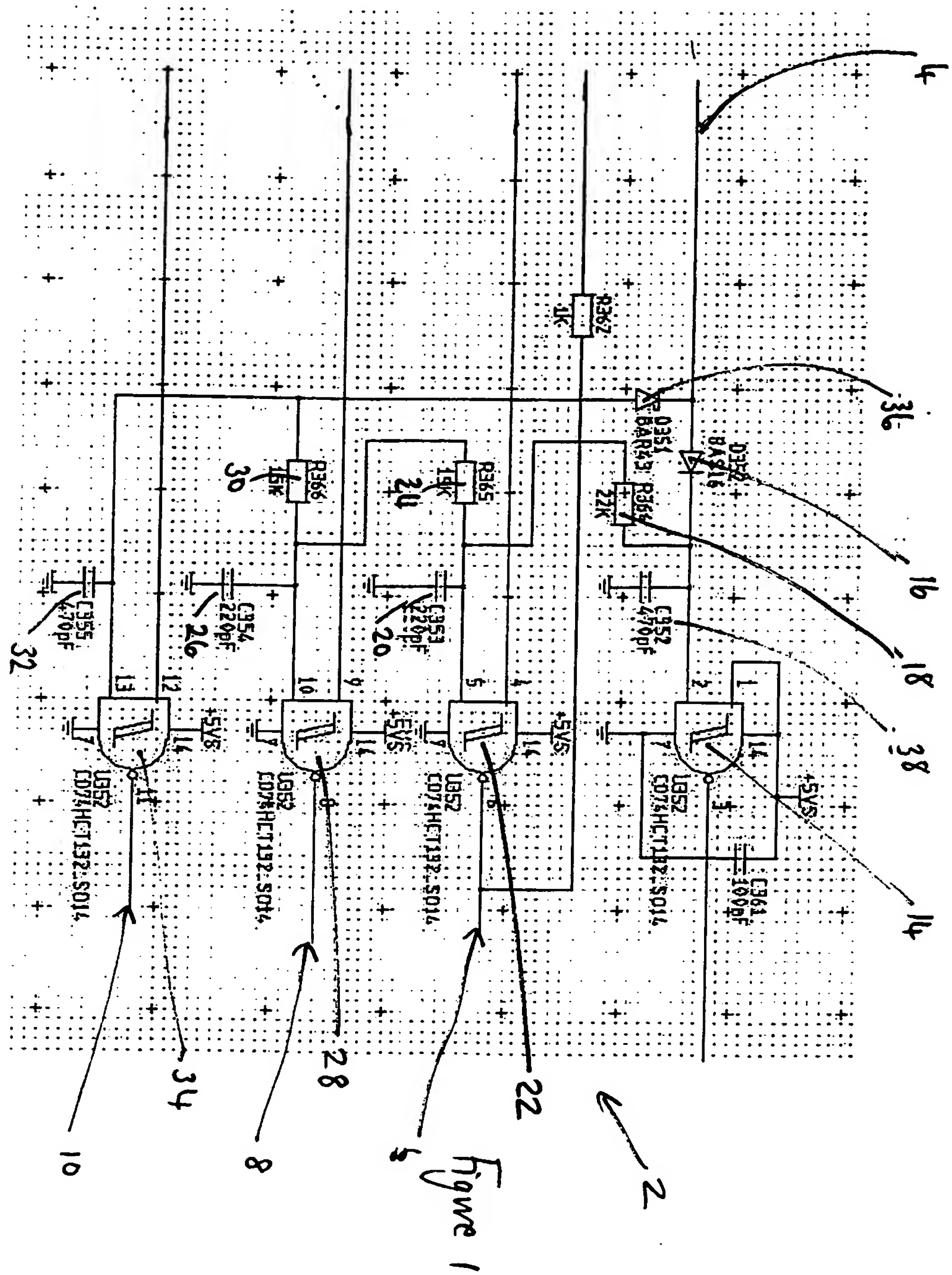
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Figure 1